Aiming at the core of the problem, **Reuse-Based Methodologies and Tools in the Design of Analog and Mixed-Signal Integrated Circuits** presents a framework for the reuse-based design of AMS circuits. The framework is founded on three key elements:

(1) a CAD-supported hierarchical design flow that facilitates the incorporation of AMS reusable blocks, reduces the overall design time, and expedites the management of increasing AMS design complexity;

(2) a complete, clear definition of the AMS reusable block, structured into three separate facets or views: the behavioral, structural, and layout facets, the first two for top-down electrical synthesis and bottom-up verification, the latter used during bottom-up physical synthesis;

(3) the design for reusability set of tools, methods, and guidelines that, relying on intensive parameterization as well as on design knowledge capture and encapsulation, allows to produce fully reusable AMS blocks.

Reuse-Based Methodologies and Tools in the Design of Analog and Mixed-Signal Integrated Circuits features a very detailed, tutorial, and in-depth coverage of all issues and must-have properties of reusable AMS blocks, as well as a thorough description of the methods and tools necessary to implement them. For the first time, this has been done hierarchically, covering one by one the different stages of the design flow, allowing us to examine how the reusable block yields its benefits, both in design time and correct performance.

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Castro-López · Fernández
Guerra-Vinuesa · Rodríguez-Vázquez

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R. Castro-López
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Reuse-Based Methodologies and Tools in the Design of Analog and Mixed-Signal Integrated Circuits

by

R. CASTRO-LÓPEZ
IMSE-CNM-CSIC,
Spain

F.V. FERNÁNDEZ
University of Seville, IMSE-CNM-CSIC,
Spain

O. GUERRA-VINUESA
University of Seville,
Spain

and

Á. RODRÍGUEZ-VÁZQUEZ
University of Seville,
Spain

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Rafael Castro López

To my family and friends

Francisco V. Fernández

To Eli, Judit, and Nuria

Óscar Guerra Vinuesa

To my wife and daughters

Ángel Rodríguez Vázquez

To my former doctoral students and current friends

Contents

Preface

Whether the widely cited Moore's Law –forecasting that the number of transistors that can be fit into a chip roughly doubles every two years– has actually represented a roadmap the semiconductor industry has struggled to comply with or a long-term prediction proven true, the fact is that this industry has accomplished spectacular breakthroughs in past decades, pervasively impacting most aspects of everyday life.

Despite these breakthroughs, the spiraling cost of integrated circuit (IC) design is slowly but surely wrapping a noose around the neck of the semiconductor industry. The economics of building today's even-more-complex ICs under even-more-stringent time-to-market requirements (perhaps the most impelling forces in modern semiconductor industry) are already so daunting that the 2003 ITRS report singled out the cost of chip design as "the greatest threat to the continuation of the semiconductor roadmap". The resulting design productivity gap –the gulf between what is possible to manufacture and what is possible to design– will certainly widen, slowing down this industry's phenomenal growth.

In the past, the industry has extracted itself from design cost traps by finding a way to automate portions of the IC design process, allowing designers to become more productive and driving costs back down. Today, the problem cannot be tackled by still relying on 20-year-old design automation technology or by simply hiring more qualified engineers. The design community believes that powerful computer-aided design (CAD) tools and capable CAD-based methodologies do not suffice in order to successfully and utterly bridge the design gap, but that some kind of design paradigm shift must be urgently put on stage.

In this sense, reuse-based design practices are regarded as a promising solution, and concepts such as IP Block, Virtual Component, and Design

Reuse have become commonplace thanks to the significant advances in the digital arena. Although far from being completely settled, an important market has flourished around digital reuse that furnishes design companies with solutions to noticeably improve their productivity rate.

When it comes to analog and mixed-signal (AMS) design, the scenario is, unfortunately, not that optimistic. The current level of AMS CAD, lagging several generations behind digital design automation partly because of the very nature of AMS design –more subtle, hierarchically loose, and handicraft-demanding–, partly because of the comparatively smaller amount of R&D dedicated to AMS CAD, and the huge heterogeneity of AMS circuits, has so far hindered a similar level of consensus and development on AMS reuse-based design, frequently influencing the idea that inheriting digital reuse concepts is impractical or simply unrealizable. It is necessary to remark, however, the importance of improving AMS design productivity: despite the relatively smaller silicon area dedicated to AMS circuitry, the time needed to design this circuitry dominates, in most cases, the total design time. Therefore, any research ultimately targeted at the improvement of the design productivity of ICs should consider AMS design productivity as a goal priority as well. Otherwise, design productivity will eventually get stuck on the AMS design bottleneck.

In this scenario, the research reported in this book tries to demonstrate not only that reuse-based design in the AMS arena is possible, but also that by following such a design paradigm and making use of appropriate CAD tools, techniques, and methods, it is possible to break through the bottlenecks of AMS design and enhance the design productivity. The concept of reuse here cannot be simply based on plug-in pre-designed, fixed circuit blocks out of a design repository, but rather on recycling these blocks; that is, adopting a flexible methodology by which a circuit can be easily and seamlessly adapted to different design specifications, different environments, and different technology nodes and foundries, thereby completing a AMS design project in time.

This book presents a framework for the reuse-based design of AMS integrated circuits. This framework is founded on three key elements:

- first, a CAD-supported hierarchical design flow that facilitates the incorporation of AMS reusable blocks. Thanks to this design reuse flow, overall design time can be reduced and increasing AMS design complexity can be efficiently managed;
- second, a complete and clear definition of the AMS reusable block. Such definition is structured into three separate facets or views: the

behavioral, structural, and layout facets. Throughout block reuse, design information flows from one facet to another, progressively adapting it to the targeted performance and technology. Each facet is devised to suit a stage of the design reuse flow, at its corresponding hierarchical level. In this way, the behavioral and structural facets are used for top-down electrical synthesis and bottom-up verification, and the layout facet is used for bottom-up physical synthesis;

- third, the set of methods, tools, and guidelines composing the design for reusability methodology, which allows producing fully reusable AMS blocks. This methodology relies on intensive facet parameterization as well as on the capture and encapsulation of design knowledge within each facet.

Although the book undertakes the problem from a general perspective, covering all different stages of the design flow, it makes special emphasis on AMS physical design reuse, as this is one of the most (if not the most) crucial, knowledge-intensive stages of the AMS design flow, thus posing a greater challenge to reuse-based design.

The framework is completed with a synthesis technique that aims at speeding up the design process of AMS ICs by reducing the time-consuming, error-prone iterations between electrical and physical synthesis, traditionally considered as non-miscible design stages. In this so-called layout-aware electrical synthesis, a simulation-based optimization algorithm explores the design space while specific and detailed information of the circuit layout –its geometric features and its layout-induced degradation on the circuit's performance– is used to improve the synthesized solution, yielding a correct-by-construction physical implementation of the circuit during the first pass.

The framework has been put into practice and assessed on a well-known, commercial design environment (*Design Framework II* from Cadence®). Furthermore, the framework has been validated through an industrial-scale, functional silicon prototype, consisting in an universal IQ transmit interface for wireless communications.

The contents of this book are organized in seven chapters as follows.

Chapter 1 introduces the problem rationale by examining the evolution of the semiconductor industry, analyzing the current challenges, and delving into the causes of the design productivity gap. To set the background of the research, the chapter then proceeds to clearly define the problem by resorting to several key concepts such as hierarchy, abstraction level, and circuit view, and answering the question of why traditional AMS design methodologies cannot solve it.

Chapter 2 reviews the current state of AMS design automation technology and, in the light of this revision, presents the reuse-based design paradigm. The digital reuse scenario is then examined in order to give insight into the differing requirements of AMS reuse. Afterwards, the chapter surveys the state-of-the-art of AMS reuse-based design. Last, the reuse-based design framework proposed in this book is described.

Chapters 3, 4, and 5 respectively describe the behavioral, structural, and layout facets of the AMS reusable block. The description of each facet follows a three-part structure: what is and what is the facet used for, what requirements does reuse-based design impose on the facet, and how reusability can be built on the facet. Accompanying the descriptions, each chapter contains detailed illustrative examples.

Chapter 6 reports the experimental demonstration of the validity of the reuse-based design framework. This chapter comprises several design experiments, as well as the description and experimental verification results of the silicon prototype mentioned above, whose analog section has been designed under the proposed framework.

Finally, Chapter 7 presents and demonstrates the layout-aware synthesis technique.

The considerations presented in Chapters 4, 5, and 7 are complemented in Appendix A.

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Chapter 1

Introduction

1 PROBLEM OVERVIEW: THE DESIGN GAP

Nowadays, the semiconductor industry and the design community are facing some very exciting and difficult challenges. For this industry to continue with its phenomenal historical growth and the well-known Moore's law, advances in all fronts are necessary. Although the integration of more and more functionalities onto a single chip is being proven as an effective strategy in terms of fabrication costs, the design effort has been continuously increasing. Both tightening time-to-market pressures and increasing design complexity are widening the gap between the available number of transistors and the ability to design them. This is even more pronounced in the area of analog and mixed-signal design, since design automation is still very far from its digital counterpart. Furthermore, analog and mixed-signal design methodologies are unable to cope with time-to-market and design complexity, the two fundamental forces driving the semiconductor industry.

In this chapter, the problem is investigated and properly defined and for that purpose this section provides the main motivations of the research reported in the book. First, an overview of the evolution of the semiconductor industry is given to set the background. Then, the design gap problem is discussed and, finally, the impact on analog and mixed-signal design is analyzed.

1.1 Evolution of the semiconductor industry

In the nineteenth century, there were more technology achievements than in the nine centuries preceding it. Then, in the first twenty years of the twentieth century, we saw more advancement than in all of the nineteenth century. Now, paradigm shifts occur in only a few years' time. In the twenty-first century, it is expected that there will be almost 1000 times greater technological changes than in its predecessor. This fact also holds true for the industry of microelectronics, which, in the past 40 years, has experimented an incredible and rapid improvement in its products. Multiple evidences of this development are all around us. Semiconductor devices are becoming smaller, almost disappearing into the background. Computational power derived is being applied to many areas of human experience: communications, data storage, medicine, genomics, and so on. The electronic industry is now one of the largest industries in terms of output as well as employment in many nations. The importance of electronics in the economic, social, and even political development throughout the world will no doubt continue to increase.

Semiconductor devices have long been used in electronics. By 1947, the physics of semiconductors was sufficiently understood to allow Brattain and Bardeen to create an amplifying circuit utilizing a point-contact "transfer resistance" device that later became known as a transistor. In 1958, Kilby created the first integrated circuit (IC), ushering in the era of modern semiconductor industry.

The sustained growth of electronics has resulted principally from the industry's ability to decrease exponentially the minimum feature size it uses to fabricate integrated circuits, commonly referred as Moore's Law[1]. Gordon Moore made his famous observation in 1965, just six years after the first planar integrated circuit was completed. The press called his analysis the "Moore's Law", and the name has stuck. In his original paper [Moore65], Moore observed an exponential growth in the number of transistors per integrated circuit and predicted that this trend would continue. In his own words:

> *The complexity for minimum component costs has increased at a rate of roughly a factor of two per year [...] Certainly over the short term this rate can be expected to continue, if not to increase. Over the longer term, the rate of increase is a bit more uncertain, although there is no reason to believe it will not remain nearly constant for at least 10 years. That means by 1975, the number of components per integrated circuit for minimum cost will be 65,000.*

That is, Gordon Moore predicted that the number of transistors that can be fit into a chip would roughly double every year. Later, in 1975, he updated this figure, so the prediction was that the number of transistors would double every two years [Moore75]. The plot in Fig. 1 illustrates this progress. It

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[1] This Law actually refers to digital circuits implementing dynamic memories (DRAM), whose topological regularity allows a higher integration capacity, thus giving an idea of the maximum number of transistors that can be integrated in a given fabrication technology.